AMENDMENTS TO THE SPECIFICATION:

Please insert on page 1, after the title, the following paragraph:

--The present Application is a continuation Application of prior U.S. Application No. 10/260,947, filed September 30, 2002, which in turn is a Divisional of U.S. Application No. 09/910,994, filed July 23, 2001, now U.S. Patent No. 6,514,852, issued February 4, 2003.--

Please replace the paragraph beginning on page 2, line 2, with the following rewritten paragraph:

--Referring to Figs. 1A ~~to 1A~~ to 1H, a conventional method (hereinafter referred to as "the first conventional method") for the formation of the low-K layer as the interlevel dielectric film and the embedded interconnection structure based on the dual damascene technique will be described. These figures are sectional views consecutively illustrating the respective steps of the process for formation of the embedded interconnection structure by using the first conventional method.--

Please replace the paragraph beginning on page 20, line 25, with the following rewritten paragraph:

--Then, as shown in Fig. 7J, the P-SiO_2 film 152, the low-K layer 148, and the P-SiO_2 film 146 are selectively etched by using the P-SiN film 154 as an etching mask and a mixture of N_2 and H_2 gases as an etching gas, thereby forming third openings ~~66A~~ 166A which expose the P-SiC film 144 therethrough.--

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